IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicant : Joseph M. Brand
Title : ENCAPSULANT LOCK FEATURE
Docket No. : MIO 0051 V2

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

This preliminary amendment is being filed to add the claims below. Please enter this amendment prior to any Office Actions. Examination and favorable consideration are respectfully requested.

In the Specification

Attached hereto as Appendix A is a marked up reproduction of the changes made to the specification and claims by the current amendments. Additions have been underscored and deletions have been bracketed.

Please replace the title of this invention with the following new title:

--METHOD OF FABRICATING AN ENCAPSULANT LOCK FEATURE IN INTEGRATED CIRCUIT PACKAGING--

At page 1 after the Title, please insert the following:

--CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. Patent Application Serial No. 09/694, 412, filed October 23, 2000, which is a division application of U.S. Patent Application Serial No. 09/335,618, filed June 18, 1999.--

In the Claims

The entire set of presently pending claims has been reproduced below for the convenience of the Examiner. Amended claims and new claims are indicated as such in the parenthetical following each claim number. Additionally, please cancel claims 31, 35-39, and 46-49.

30. A method of encapsulating an integrated circuit comprising the steps of:

providing a semiconductor chip;

providing a laminate defining first and second major faces, said laminate including an electrically conductive layer, and an underlying substrate supporting said electrically conductive layer;

forming at least one void in said laminate so as to extend from one of said major faces through said electrically conductive layer at least as far as said underlying substrate; and

encapsulating said semiconductor die and said laminate with an encapsulant such that said encapsulant extends into said void to contact said underlying substrate.

32. A method of forming a laminate to lock an encapuslant comprising:

providing a first laminate layer;

forming a second laminate layer over the first laminate layer, so as to define an underlying cavity;

forming a third laminate layer over the second laminate layer, so as to define a void portion over the underlying cavity;

forming a fourth laminate layer over the third laminate layer, so as to define a void portion over the void portion of the third laminate layer;

forming a conductive layer over the fourth laminate, so as to define a void portion over the void portion of the fourth laminate layer; and

forming a solder resist layer over the conductive layer, so as to define a void portion over the void portion of the conductive layer.

33. The method of claim 32, wherein the underlying cavity, the void portion of the third laminate layer, the void portion of the fourth laminate layer, the void portion of the conductive layer and the void portion of the solder resist layer are formed to collectively form a void.

34. The method of claim 33 further comprising:

placing a die over at least a portion of the solder resist layer;

forming an encapsulant over the solder resist layer, over the die and in the void.

40. A method of encapsulating an integrated circuit comprising:

providing a die;

providing a substrate having at least one resin layer;

forming at least one laminate layer over the at least one resin layer;

forming a void in the at least one resin layer and the at least one laminate layer such that a portion of the void located in the at least one resin layer is below a remaining portion of the at least one laminate layer;

placing the die over the at least one laminate layer; and

encapsulating the die by forming encapsulant over the at least one laminate layer, over the die and in the void.

41. The method of claim 40, wherein the at least one laminate layer is formed by forming a conductive layer over the at least one resin layer and forming a solder resist layer over the conductive layer.

42. The method of claim 40, wherein the void is formed by forming an underlying cavity in the at least one laminate layer.

43. The method of claim 40, wherein the encapsulant is formed in substantially all of the void.

44. The method of claim 40, wherein the at least one resin layer is formed from bismaleimide triazine laminate.

45. The method of claim 40, wherein the at least one resin layer is formed from FR-4 epoxy-glass laminate.

50. (New) The method of claim 33, wherein the void has a varying profile.

51. (New) The method of claim 50, wherein the void having a varying profile is formed by a process selected from the group consisting of drilling, stamping, chemical etching, and combinations thereof.

52. (New) The method of claim 50, wherein the void having a varying profile is formed having a T-shaped profile.

REMARKS

Claims 30, 32-34 and 40-45 were subject to a restriction requirement in the related application. Claims 31, 35-39, and 46-49 are cancelled. Claims 50-52 have been added. Thus, claims 30, 32-34, 40-45, and 50-52 are now pending.

The title of the invention is amended to better describe the present invention. Additionally, the specification is amended to indicate related application information consistent with US patent practice.

The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this amendment. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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& SCHAEFF, L.L.P.

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APPENDIX - A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The title has been amended as follows:

--[ENCAPSULANT LOCK FEATURE] METHOD OF FABRICATING AN ENCAPSULANT LOCK FEATURE IN INTEGRATED CIRCUIT PACKAGING--